WHAT IS CLAIMED IS:

1. A method for modeling a device and a network to be analyzed in a complex simulation for analyzing, in a complex fashion, a semiconductor device and a network that includes the device, the method comprising:

a device extraction step for extracting the structure of each of a plurality of devices included in the network to create device models showing the individual extracted structures;

a device connection step for connecting the respective device models through the intermediary of an insulating portion for cutting off the electrical connection between the respective device models; and

a circuit connection step for connecting a network model showing the network portion, from which the plurality of devices extracted in the device extraction step have been excluded, to a predetermined device model among the connected device models.

2. The modeling method according to Claim 1, wherein, in the device extraction step, two-dimensional models showing the sectional structures of the individual corresponding devices are used as the device models.

3. The modeling method according to Claim 1, wherein, in the device extraction step, the models showing the three-dimensional structures of the corresponding devices are used

as the device models.

4. The modeling method according to Claim 1, wherein, in the device connection step, the device models are connected through the conducting portions that permit partial conduction among the device models to be connected.

5. The modeling method according to Claim 1, wherein, in the device connection step, space portions are formed to provide a gap between device models to be connected.

6. The modeling method according to Claim 1, further comprising an electrode potential setting step for setting potentials, which are different from each other, at predetermined multiple potential points in an electrode of a device model to which the network portion has been connected.